

REMARKS

By the present amendment and response, independent claims 16 and 34 have been amended to overcome the Examiner's objections. Claims 16-34 are pending in the present application. Claims 28-33 have been allowed. Reconsideration and allowance of pending claims 16-27 and 34 in view of the following remarks are requested.

The Examiner has rejected claims 16-20, 23, 24, 26, and 34 under 35 USC §102(e) as being anticipated by U.S. patent number 6,222,269 to Usami ("Usami"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 16 and 34, is patentably distinguishable over Usami.

The present invention, as defined by amended independent claim 16, teaches, among other things, an interconnect comprising one or more metal lines formed from a first metal layer, where the metal lines have gaps therebetween, a low-k material filling the gaps between the metal lines and having a height and one or more vertical portions, a protective layer formed directly over the metal lines and the low-k material, where the protective layer covers at least one vertical portion of the low-k material, and a dielectric layer formed over the protective layer, where the dielectric layer has a different composition than the low-k material and the protective layer. As disclosed in the present application, the protective layer formed directly over the metal lines and the low-k material that is situated between the metal lines provides an etch stop that protects the low-k material from chemicals utilized to etch vias in the dielectric layer situated above

the metal lines. As such, the protective layer prevents the undesirable formation of poisoned vias that can occur when the low-k material situated in gaps between the metal lines is exposed to chemicals utilized to etch the vias. Thus, by utilizing low-k material situated in gaps between metal lines and a protective layer directly over the metal lines and the low-k material, the present invention advantageously achieves an interconnect having reduced interconnect capacitance without suffering the undesirable effects of poisoned vias.

In contrast, Usami does not teach, disclose, or suggest an interconnect comprising, among other things, a low-k material filling gaps between metal lines formed from a first metal layer, a protective layer formed directly over the metal lines and the low-k material, and a dielectric layer formed over the protective layer, where the dielectric layer has a different composition than the low-k material and the protective layer. Usami specifically discloses an interconnect comprising a plurality of lower interconnect lines 3 formed on first stopper layer 2, which is formed on thick insulating layer 1 on the surface of a semiconductor substrate. See, for example, column 5, lines 55-65 and Figure 1 of Usami. First interlevel insulator 4 is formed in a widely spaced region between adjacent lower interconnect lines 3, while low dielectric constant layer 5 is formed in a narrowly spaced region between adjacent lower interconnect lines 3. See, for example, column 5, lines 66-67, column 6, lines 1-2 and Figure 1 of Usami. Thus, in Usami, low dielectric constant layer 5 is formed only in narrowly spaced regions between adjacent lower interconnect lines 3. In Usami, an interlevel insulator having a small coefficient of thermal expansion

and high strength is used in the widely spaced region between interconnect lines to overcome the problem of crack generation which would take place if a low-dielectric constant insulating layer were used in all the regions (both widely and narrowly spaced regions) as an interlevel insulator. See, for example, Usami, column 8, lines 21-27. Thus, Usami teaches against using a low dielectric constant layer in all of the regions between interconnect lines.

In Usami, second interlevel insulator 6 is situated over interconnect lines 3, first interlevel insulator 4, and low dielectric constant insulating layer 5. See, for example, column 6, lines 10-13 and Figure 1 of Usami. Second stopper layer 7 is situated over second interlevel insulator 6, and third interlevel insulator 8 is situated over second stopper layer 7. See, for example, column 6, lines 10-13 and Figure 1 of Usami. Second interlevel insulator 6 and third interlevel insulator 8 are composed of silicon dioxide or the like having a low hygroscopicity. See, for example, Usami, column 6, lines 18-21. Thus, in Usami, a dielectric layer, i.e. second interlevel insulator 6, is situated directly over interconnect lines 3, first interlevel insulator 4, and low dielectric constant insulating layer 5, and a protective layer, i.e. second stopper layer 7, is situated over second interlevel insulator 6. In a second embodiment, protective insulating layer 17 is formed between lower interconnect lines and low dielectric constant insulating layers 5. See, for example, column 8, lines 56-59 and Figure 5. In the second embodiment, as shown in Figure 5, protective insulating layer 17 is not situated over low dielectric constant insulating layers 5. For the foregoing reasons, Applicant respectfully submits that the

present invention, as defined by amended independent claim 16, is not suggested, disclosed, or taught by Usami. As such, the present invention, as defined by amended independent claim 16, is patentably distinguishable over Usami. Thus, claims 17-20, 23, 24, and 26 depending from amended independent claim 16 are also patentably distinguishable over Usami.

The present invention, as defined by amended independent claim 34, teaches, among other things, a material filling gaps between a plurality of metal lines formed from a first metal layer, a protective layer formed directly over the metal lines and the material, and a dielectric layer formed over the protective layer, where the dielectric layer has a different composition than the protective layer. For similar reasons as discussed above, the invention, as defined by amended independent 34, is also patentably distinguishable over Usami.

The Examiner has further rejected claims 21, 22, 25, and 27 under 35 USC §103(a) as being unpatentable over Usami. As discussed above, amended independent claim 16 is patentably distinguishable over Usami and, as such, dependent claims 21, 22, 25, and 27 are, a fortiori, also patentably distinguishable over Usami.

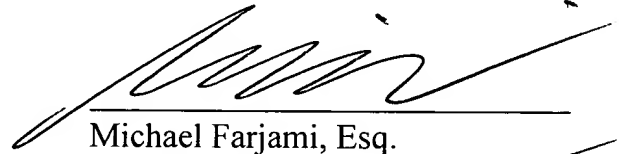
Based on the foregoing reasons, the present invention, as defined by amended independent claims 16 and 34 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 16-27 and 34 pending in the present application are patentably distinguishable over the art cited by the Examiner.

For all the foregoing reasons, an early Notice of Allowance directed to the already allowed claims 28-33 as well as pending claims 16-27 and 34 is respectfully requested.

It is noted that **Applicant's attorneys have changed** and a copy of the "Revocation and Power of Attorney" already filed in the present application is attached hereto for the Examiner's reference. The Examiner is respectfully requested to correspond with Applicant's new attorneys whose contact information appears below.

Respectfully Submitted,
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Date: 10/4/02


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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 16 and 34 have been amended as follows:

16. (Twice Amended) An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling the gaps between the metal lines and having a height and one or more vertical portions;

(c) a protective layer formed directly over the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the low-k material and the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal vias to contact the first metal lines.

34. (Once Amended) An interconnect comprising:

(a) a plurality of metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) material filling the gaps between the metal lines and having a height and one or more vertical portions;

(c) a protective layer formed directly over the metal lines and the material, wherein the protective layer covers at least one vertical portion of the material;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal within the vias;

(g) a second metal layer formed over and in direct contact with the dielectric layer;

and

(h) one or more openings in the protective layer for allowing the metal in the vias to contact the metal lines.